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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/714,325	11/15/2000	Sung-Bae Park	SAM-169	4343

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/714,325	PARK, SUNG-BAE	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 1 has been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE as received on 12/1/04.

Specification

3. The disclosure is objected to because of the following informalities: In the amended paragraph beginning on page 6, line 8, it is not clear how an address trace cache is composed of a start address and an end address for respectively storing routine start and end addresses. That is, how does an address store an address? Applicant should clarify this by saying that the trace cache comprises start address storage for storing a start address (likewise, end address storage for storing the end address). Also, if any other instances of this occur, please correct them.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 1 recites the limitation "the environment" in line 2. There is insufficient antecedent basis for this limitation in the claim. The examiner recommends replace "the environment of branch prediction" with --a branch prediction environment--.

7. Claim 1 recites the limitation "a start address" in the second to last line of the claim. There is insufficient antecedent basis for this limitation in the claim, as it is not clear whether or not applicant is referring to the same start address claimed in line 7.

8. Claim 1 recites the limitation "the routine" in the second to last line of the claim. There is insufficient antecedent basis for this limitation in the claim, as it is not clear whether applicant is referring to the first routine or second routine.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rotenberg et al., "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching," Proc. of the 29th International Symposium on Microarchitecture, Dec. 1996 (as applied in the previous Office Action and herein referred to as Rotenberg), in view of Nair, U.S. Patent No. 6,304,962, and further in view of Gabzdyl et al., U.S. Patent No. 6,145,076 (herein referred to as Gabzdyl).

11. Referring to claim 1, Rotenberg has taught a method of executing instructions using an address trace cache in the environment of branch prediction comprising the steps of:

a) if a first routine composed of a first group of instructions is to be executed, storing each instruction in the address trace cache according to an order of executed instructions. See Fig.2, and note the dynamic instruction stream, which is composed of routines with unrepeated and/or repeated instructions in the order of execution. Furthermore, see Fig.2 and page 25, column 1, 2nd paragraph under section 1.1. Rotenberg has not taught storing the instruction addresses in the address trace cache. However, Nair has taught a component called a Superblock Target Buffer (STB), which acts like a common trace cache in that it tries to predict long execution paths. However, unlike a common trace cache, the STB stores instruction addresses and not the instructions themselves. See column 10, lines 11-17. Official Notice is taken that address sizes may be less than instruction sizes, and consequently, it would have been obvious to one or ordinary skill in the art at the time of the invention to modify Rotenberg such that the address trace cache stores instruction addresses as opposed to the instructions themselves. Doing so would allow more items to be stored. In addition, it should be realized that it is not necessarily important whether instructions or instruction addresses are stored in a trace cache. Instead, all that is required is that instructions may be identified by the trace cache and this may be done by providing the instruction or its address.

b) Rotenberg has not taught that if a second routine composed of a second group of instructions is to be repeatedly executed, storing a routine start address, a routine end address, a current iteration count of the routine representing a current number of executed iterations of the routine, and a total loop iteration count for storing the total number of iterations of the routine. However, Gabzdyl has taught a repeat control circuit for handling the execution of loops (Fig.5 and column 5, lines 15-23), which stores:

(i) The start address of the repeating instruction routine (element 502).

(ii) The end address of the repeating instruction routine (element 503).

(iii) The total number of iterations of the routine (element 504).

As disclosed by Gabzdyl in column 1, lines 44-54, this type of circuit is advantageous in the processing of nested loops because the completion of a first inner loop count may coincide with a plurality of outer loop counts on the same clock cycle without risk of the program instructions becoming out of step with their associated hardware. Gabzdyl provides a hardware enhancement to a processor circuit so as to relieve the burden placed upon an assembler or compiler used for converting high level code into executable instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Rotenberg such that for second routine, start and end routine addresses along with a total iteration count are stored.

c) Gabzdyl fails to teach storing a current iteration count of the routine and a current loop iteration counter for counting the current iteration count. However, it should be realized that such a component is not required by Gabzdyl because in Gabzdyl, the total iteration count is decremented until it reaches "0". Once it reaches this value, the loop is finished. The examiner asserts that Gabzdyl's system is functionally equivalent to applicant's in that while Gabzdyl's system decrements the total iteration count until it matches "0", applicant's system increments the current iteration count until it matches the total iteration count (hence, the current count must be stored in applicant's system). Both implementations offer the same functionality and are merely a design choice. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Gabzdyl to store a current iteration count and count up

as opposed to counting down because this is functionally equivalent. Finally it should be realized that applicant has not claimed storing the start and end addresses and the current and total counts in the trace cache. And, this circuit may be considered part of the trace cache.

e) Rotenberg has taught addressing a start address (Fig. 4, fall-thru and target address), which will be accessed subsequent to the routine (trace) when a trace ends. Rotenberg in view of Gabzdyl has not taught that this access will occur when the current count and total count are identical. However, when a loop ends in, instructions subsequent to the loop will inherently be accessed. Therefore, because Rotenberg has been modified in view of Gabzdyl, and Gabzdyl has taught a system that is functionally equivalent to applicant's, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to address a start address, which will be subsequent to the routine, when the values of the loop counters are identical to each other indicating the end of the routine.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
January 20, 2004

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